PEMD3; PIMD3; PUMD3

NPN/PNP resistor-equipped transistors; R1 = 10 kΩ, R2 = 10 kΩ

Rev. 09 — 18 May 2005 Product data sheet

1. Product profile

1.1 General description

NPN/PNP Resistor-Equipped Transistors (RET).

Table 1: Product overview

Type number	Package		PNP/PNP complement	NPN/NPN complement
	Philips	JEITA		
PEMD3	SOT666	-	PEMB11	PEMH11
PIMD3	SOT457	SC-74	-	-
PUMD3	SOT363	SC-88	PUMB11	PUMH11

1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

Table 2: Quick reference data

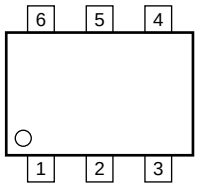
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current (DC)		-	-	100	mA
R1	bias resistor 1 (input)		7	10	13	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	

PHILIPS

2. Pinning information

Table 3: Pinning

Pin	Description	Simplified outline	Symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		



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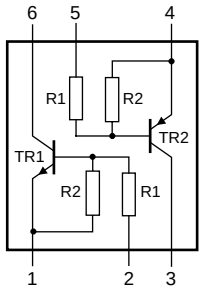

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3. Ordering information

Table 4: Ordering information

Type number	Package		
	Name	Description	Version
PEMD3	-	plastic surface mounted package; 6 leads	SOT666
PIMD3	SC-74	plastic surface mounted package; 6 leads	SOT457
PUMD3	SC-88	plastic surface mounted package; 6 leads	SOT363

4. Marking

Table 5: Marking codes

Type number	Marking code [1]
PEMD3	D3
PIMD3	M7
PUMD3	D*3

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage TR1					
	positive			-	+40	V
	negative			-	–10	V
	input voltage TR2					
	positive			-	+10	V
	negative			-	–40	V
I_O	output current (DC)			-	100	mA
I_{CM}	peak collector current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	SOT363		[1]	-	200	mW
	SOT457		[2]	-	300	mW
	SOT666		[1] [3]	-	200	mW
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	SOT363		[1]	-	300	mW
	SOT457		[2]	-	600	mW
	SOT666		[1] [3]	-	300	mW

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB with 65 µm copper strip line, standard footprint.

[3] Reflow soldering is the only recommended soldering method.

6. Thermal characteristics

Table 7: Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	SOT363		[1]	-	-	625	K/W
	SOT457		[2]	-	-	417	K/W
	SOT666		[1] [3]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	SOT363		[1]	-	-	416	K/W
	SOT457		[2]	-	-	208	K/W
	SOT666		[1] [3]	-	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB with 65 µm copper strip line, standard footprint.

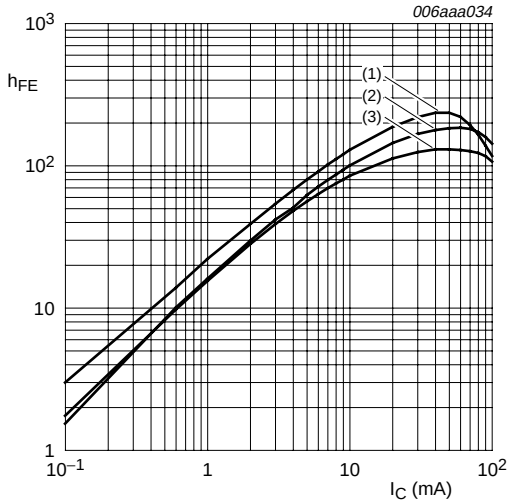
[3] Reflow soldering is the only recommended soldering method.

7. Characteristics

Table 8: Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A	-	-	1	µA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C	-	-	50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A	-	-	400	µA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA	30	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	-	-	150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA	-	1.1	0.8	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 10 mA	2.5	1.8	-	V
R1	bias resistor 1 (input)		7	10	13	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz	-	-	-	
	TR1 (NPN)		-	-	2.5	pF
	TR2 (PNP)		-	-	3	pF



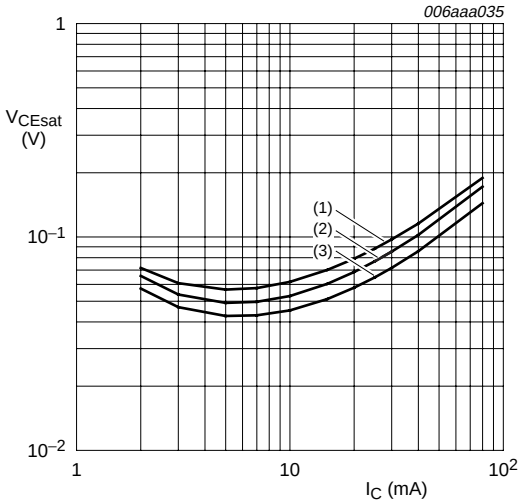
V_{CE} = 5 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = –40 °C

Fig 1. TR1 (NPN): DC current gain as a function of collector current; typical values



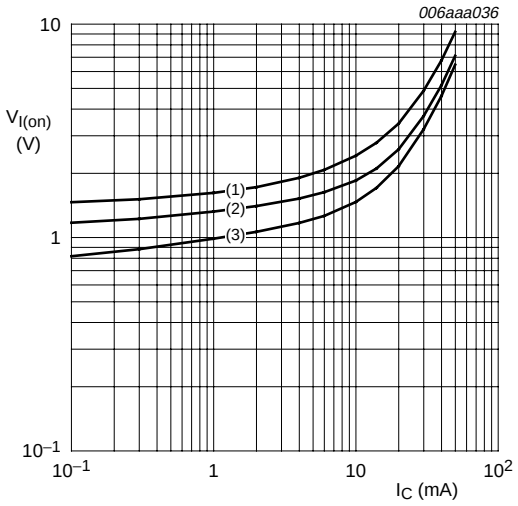
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = –40 °C

Fig 2. TR1 (NPN): Collector-emitter voltage as a function of collector current; typical values



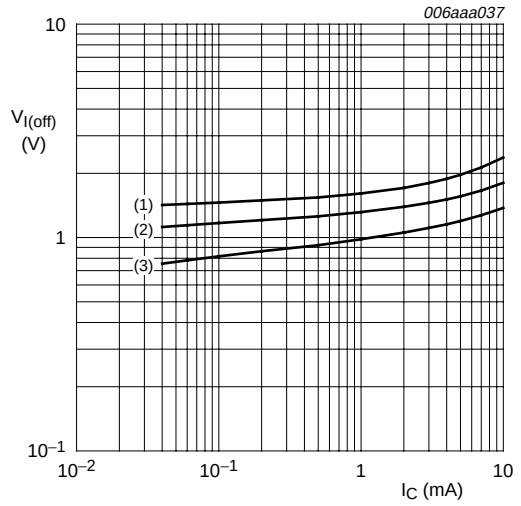
V_{CE} = 0.3 V

(1) T_{amb} = –40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 3. TR1 (NPN): On-state input voltage as a function of collector current; typical values



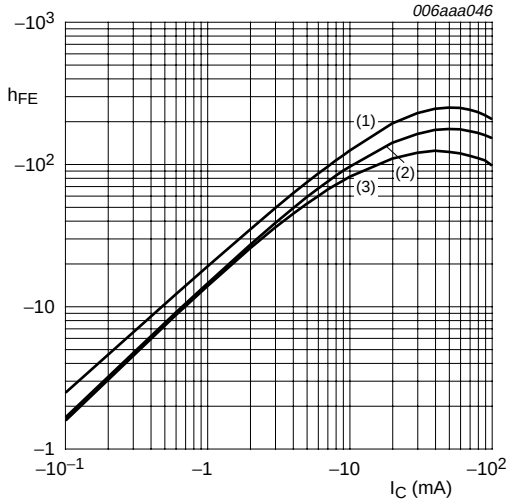
V_{CE} = 5 V

(1) T_{amb} = –40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 4. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



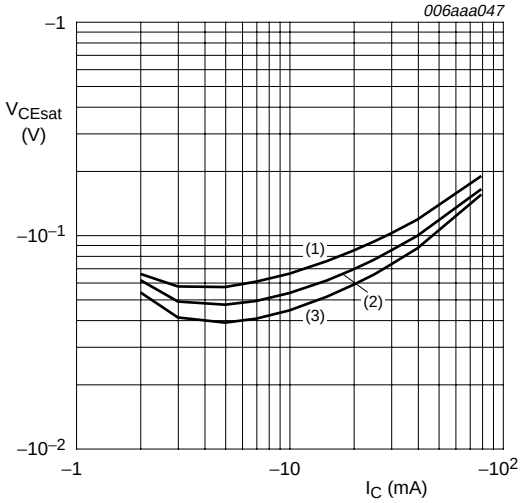
V_{CE} = −5 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 5. TR2 (PNP): DC current gain as a function of collector current; typical values



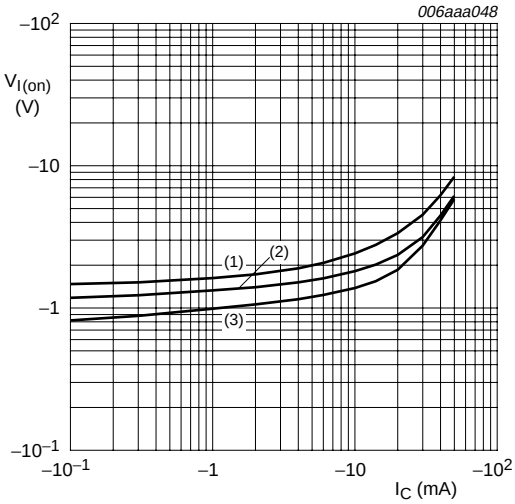
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 6. TR2 (PNP): Collector-emitter voltage as a function of collector current; typical values



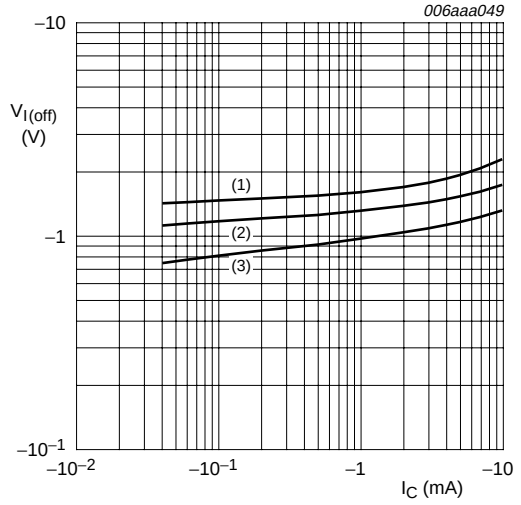
V_{CE} = −0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 7. TR2 (PNP): On-state input voltage as a function of collector current; typical values



V_{CE} = −5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 8. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

8. Package outline

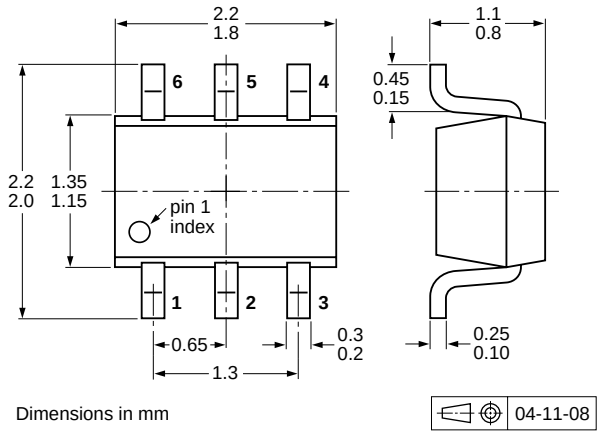


Fig 9. Package outline SOT363 (SC-88)

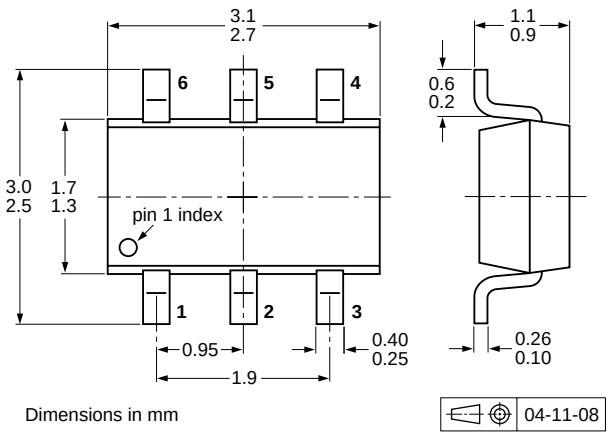


Fig 10. Package outline SOT457 (SC-74)

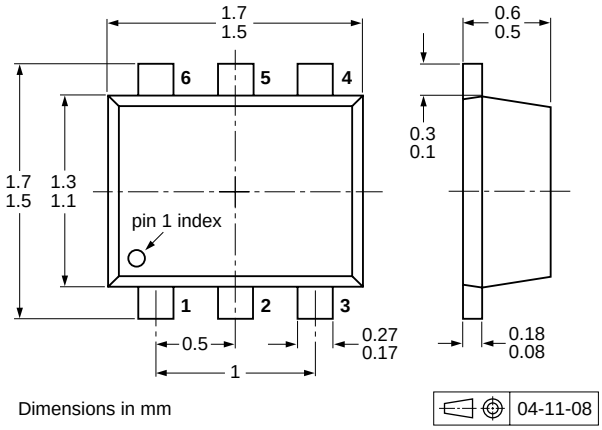


Fig 11. Package outline SOT666

9. Packing information

Table 9: Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMD3	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PIMD3	SOT457	4 mm pitch, 8 mm tape and reel; T1 [2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 [3]	-125	-	-	-165
PUMD3	SOT363	4 mm pitch, 8 mm tape and reel; T1 [2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 [3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see Section 15.

[2] T1: normal taping

[3] T2: reverse taping

10. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PEMD3_PIMD3_PUMD3_9	20050518	Product data sheet	-	9397 750 14517	PEMD3_PIMD3_PUMD3_8
Modifications:	• Table 1: EIAJ amended to JEITA • Table 9: Packing method (2 mm pitch) for SOT666 added • Section 14: added				
PEMD3_PIMD3_PUMD3_8	20041206	Product data sheet	-	9397 750 13294	PEMD3_PUMD3_7

11. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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16. Contents

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